REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the Application. Dependent Claims 3, 10 and 17 have been amended for reasons of dependency. Independent Claims 1, 8 and 15 have been amended. Dependent claims 6, 13, and 20 are cancelled without prejudice or disclaimer, and elements of which are incorporated into independent Claims 1, 8, and 15, respectively. Support for the present Amendments can be found, among other places, on in paragraph [0035], [0044] and [0046] of the present Application. Accordingly, Claims 1, 3-5, 7-8, 10-12, 14-15, and 17-19, and 21-23 are currently pending in the Application.

I. Rejection of Claims 1, 3-8, 10-15 and 17-23 under 35 U.S.C. § 103

The Examiner has rejected Claims 1, 3-8, 10-15 and 17-23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2002/0085578 A1 to Dell, *et al.* ("Dell") in view of U.S. patent No. 6,667,983 B1 to Lo, *et al.* ("Lo") and U.S. Patent No. 6,963,576 to Lee ("Lee").

Amended Claim 1 is directed to a head blockage avoidance system. The system includes a priority summarizer a priority summarizer configured to generate a priority summary of packets within m inputs and n packet FIFOs that indicates which of the n packet FIFOs is to receive a highest priority packet from one of the m inputs, *wherein each of the packet FIFOs can receive packets of two or more differing priorities*. The head avoidance blockage system further comprises a scheduler configured to cause packets in the n packet FIFOs to be queued for processing based on the priority summary such that packets in a packet FIFO that is to receive the highest priority packets are triggered to be processed before packets in other of the n packet FIFOs *so that a lower*

priority packet in the n packet FIFO is scheduled for processing before a higher priority packet concurrently contained in another of the n packet FIFOs is scheduled for processing. (Emphasis added.) The head avoidance blockage system further includes *a destination FIFO and an output, the destination FIFO interposing the n packet FIFOs and the output, the scheduler further configured to transfer at least one of the packets from the one of the m inputs toward the output only if the n packet FIFO and the destination FIFO are both available to simultaneously contain the packet.*

As discussed in the previous Amendment of May 21, 2007, Dell is directed to a switching stage that employs crossbar devices. (*See* page 2, paragraph [0013].) In Dell, the "switch fabric of the present invention is a cell-switching engine handling fixed-sized switching cells." (*See* page 6, paragraph [0090].) Dell uses one or more crossbars to achieve scalability in self-routing of cells. (*See* page 2, paragraph [0012].)

The Examiner admits that Dell arbitrates between packets based on priority such that packets in a FIFO *that contain the highest priority are always processed before packets in other FIFOs.* (*See* Examiner's Action of August 3, 2007, page 3; emphasis added.) However, in the "Argument" section of the present Examiner's Action, the Examiner contends:

> Although it is true, as argued by the Applicant, that a lower priority packet *may* be scheduled before a higher priority packet under a system as described by [previously presented] claim 1, such a situation is not required by the current language of claim 1. Thus, the claim does not require a lower priority packet to be scheduled before a higher priority packet, as argued by the Applicant. (*See* Examiner's Action, pages 9-10; emphasis in Examiner's Action).

Although the Applicants reserve the right to traverse the above argument at a later time, for

the purpose of expediting prosecution, the Applicants amend Claim 1 to explicitly recite: "a scheduler configured to cause packets in the n packet FIFOs to be queued for processing based on the priority summary such that packets in a packet FIFO that is to receive the highest priority packets are triggered to be processed before packets in other of the n packet FIFOs *so that a lower priority packet in the n packet FIFO is scheduled for processing before a higher priority packet concurrently contained in another of the n packet FIFOs is scheduled for processing.*" (Emphasis added.)

In the present Application, in one embodiment of Claim 1:

> [0046] In order to prevent head of line blockage of the packet having a high priority in the first source FIFO 310 by the packet having a low priority in the first packet FIFO 330, *the scheduler 360 would queue the first [low priority] packet FIFO 330 to be processed first.* (Emphasis added.)

In the present Application, in one embodiment of Claim 1:

> [0044] This [*i.e.,* the scheduler 360] would queue the first (low priority) packet FIFO 330 to be processed first] would allow the packet having the low priority in the first packet FIFO 330 to be transferred to the destination FIFO 336. Then, the packet having a high priority would be transmitted toward the first packet FIFO 330 and the first packet FIFO 330 would be processed next. *Thus, the head of line blockage is avoided.* (Emphasis added.)

However, as discussed above, the Examiner admits that Dell arbitrates between packets based on priority such that packets in a FIFO *that contain the highest priority are always processed before packets in other FIFOs.* (*See* Examiner's Action of August 3, 2007, page 3; emphasis added.) Therefore, Dell is an inapposite reference.

Claim 1 also recites "a priority summarizer configured to generate a priority summary of the packets within the inputs and packet FIFOs indicating which of the packet FIFOs is to receive a highest priority packet from one of the inputs...." which the Examiner admits is not disclosed by Dell. However, the Examiner cites to Lo to compensate this deficiency of Dell. The Examiner contends, regarding Lo: "...since all packets having the highest priority go to the transmit FIFI entry point circuit corresponding to the highest priority, the pointer used by Lo et al. to sort packets corresponding to the highest priority transmit FIFO entry point circuit inherently also corresponds to the transmit FIFO entry circuit that is to received *(sic.)* a highest priority packet." (*See* Examiner's Action, page 6.)

Although the Applicants again respectfully disagree with the Examiner's interpretation of the previously presented claim language of independent Claim 1, in the interests of furthering prosecution, the Applicants further amend Claim 1 to further recite that: "a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs is to receive a highest priority packet from one of said m inputs, *wherein each of said n packet FIFOs can receive packets of two or more differing priorities...*"

The Applicants respectfully disagree with the Examiner's characterization of Claim 1 as currently amended applied to the cited reference of Lo. In Lo, each entry point 410-416 of Lo has a fixed priority, which is then arbitrated by the scalable priority arbiter 420. However, Claim 1 recites: "a priority summarizer configured to generate a priority summary of said packets within

said m inputs and said n packet FIFOs that indicates *which* of said n packet FIFOs *is to receive a highest priority packet* from one of said m inputs, *wherein each of said n packet FIFOs can receive packets of two or more differing priorities...*" (Emphasis added.)

In Lo, circuit 405 of FIG. 7 provides separate transmit FIFO entry point circuit 410-416 for each different transmission priority level. (*See* col. 9, lines 31-33.) In Lo, the transmission FIFO entry point circuits 410-416 act to provide a queuing function for the data packets of their associated priority type. (*See* col. 10, lines 9-11.) Lo, however, does not disclose or suggest "a priority summarizer configured to generate a priority summary of said packets within said m inputs and said n packet FIFOs that indicates which of said n packet FIFOs is to receive a highest priority packet from one of said inputs, wherein each of said n packet FIFOs can receive packets of two or more *differing* priorities..." Instead, in Lo, the transmission FIFO entry point circuits 410-416 have packets assigned to a *single* priority level.

Moreover, Claim 1 as currently amended further recites: "a destination FIFO and an output, said destination FIFO interposing said n packet FIFOs and said output, said scheduler further configured to transfer at least one of said packets from one of said m inputs toward said output *only when both said n packet and said destination FIFO are both available to simultaneously contain said packet*" which incorporates elements from cancelled dependent Claim 6, and adds further elements. (Emphasis added.) The Applicants may respectfully disagree with the Examiner's characterization of Claim 6 as pertaining to Dell as discussed in the Examiner's Action, page 8, and the Applicants respectfully reserve the right to traverse these characterizations

at a later time. Nonetheless, assuming, *arguendo*, that the Examiner is correct in this characterization of Claim 6 as pertaining to Dell, the Applicants have not found within the cited elements of Dell a destination FIFO and an output, the destination FIFO interposing said n packet FIFOs and said the ouput, and a scheduler further configured to transfer at least one of said packets from said one of said n packet FIFOs toward said destination FIFO for transmission via said output *only when both the n packet FIFO and the destination FIFO are both available to simultaneously contain said packet,* as is claimed in currently amended Claim 1. (Emphasis added.)

The Applicants have not found the above elements as claimed in Claim 1 in the cited portions of Dell or Lo. Nor has the Examiner cited Lee as curing the deficiencies of Dell or Lo regarding the arguments of Claim 1 as currently amended. Therefore, the Examiner has not presented a *prima facie* case of rejection of Claim 1. In view of the foregoing remarks, the cited references do not support of the Examiner's rejection of independent Claim 1, nor for similar reasons the rejection of independent Claim 8 and Claim 15, nor their dependent claims, when considered as a whole. Therefore, Claims 3-8, 10-15, and 17-20 are nonobvious over the cited references under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection of Claims 1, 3-8, 10-15, and 17-23 and allow issuance thereof.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this Application to be in condition for allowance and therefore earnestly solicit s a Notice of Allowance for Claims 1, 3-5, 7-8, 10-12, 14-15, 17-19, and 21-23. Furthermore, the Applicant reserves the right to address arguments and positions in the Examiner's Action at a later date that are not addressed in the present Amendment.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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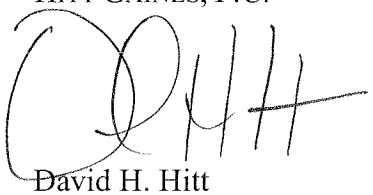

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Date: FEBRUARY 22, 2008

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